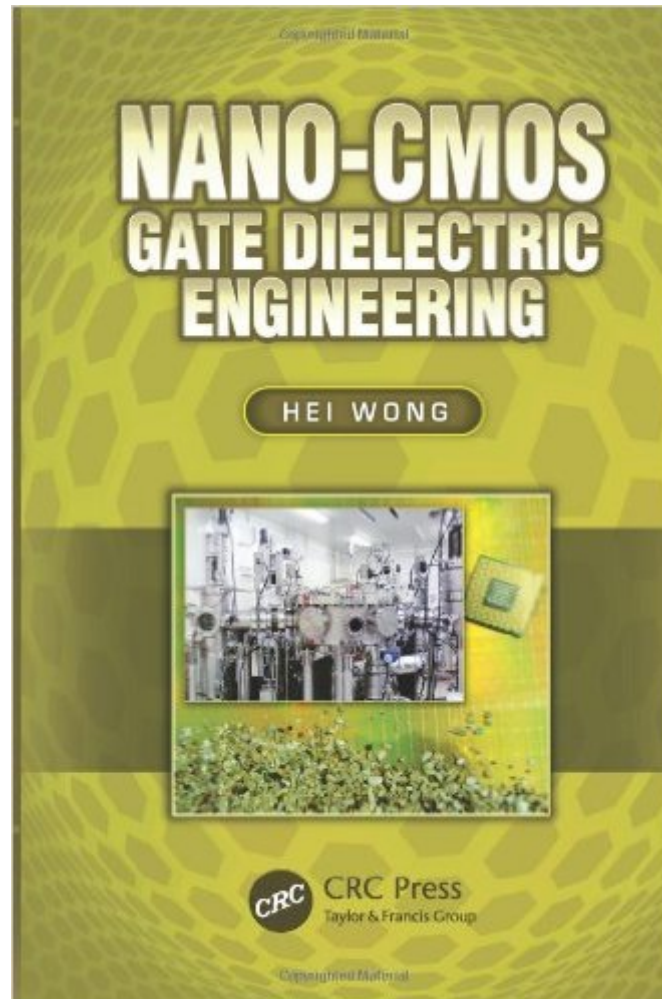


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# Nano-CMOS Gate Dielectric Engineering



## Synopsis

According to Moore's Law, not only does the number of transistors in an integrated circuit double every two years, but transistor size also decreases at a predictable rate. At the rate we are going, the downsizing of CMOS transistors will reach the deca-nanometer scale by 2020. Accordingly, the gate dielectric thickness will be shrunk to less than half-nanometer oxide equivalent thickness (EOT) to maintain proper operation of the transistors, leaving high-k materials as the only viable solution for such small-scale EOT. This comprehensive, up-to-date text covering the physics, materials, devices, and fabrication processes for high-k gate dielectric materials, Nano-CMOS Gate Dielectric Engineering systematically describes how the fundamental electronic structures and other material properties of the transition metals and rare earth metals affect the electrical properties of the dielectric films, the dielectric/silicon and the dielectric/metal gate interfaces, and the resulting device properties. Specific topics include the problems and solutions encountered with high-k material thermal stability, defect density, and poor initial interface with silicon substrate. The text also addresses the essence of thin film deposition, etching, and process integration of high-k materials in an actual CMOS process. Fascinating in both content and approach, Nano-CMOS Gate Dielectric Engineering explains all of the necessary physics in a highly readable manner and supplements this with numerous intuitive illustrations and tables. Covering almost every aspect of high-k gate dielectric engineering for nano-CMOS technology, this is a perfect reference book for graduate students needing a better understanding of developing technology as well as researchers and engineers needing to get ahead in microelectronic engineering and materials science.

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